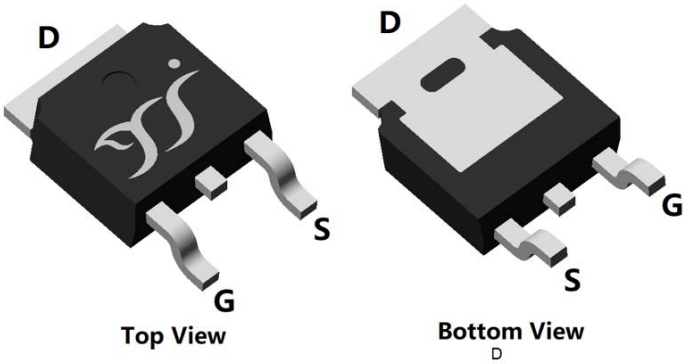
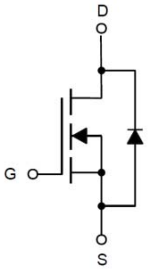
N-Channel Enhancement Mode Field Effect Transistor



TO-252



Product Summary

- V_{DS} 100V
- I_D 45A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜17mΩ
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜21.5mΩ
- 100% UIS Tested
- 100% ▽V_{DS} Tested

General Description

- Low $R_{DS(on)}$ & FOM
- Extremely low switching loss
- Excellent stability and uniformity
- Fast switching and soft recovery
- Part no. with suffix “Q” means AEC-Q101 qualified

Applications

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply
- DC-DC convertor

■ Absolute Maximum Ratings (T_A=25℃ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_A=25℃	I_D	7	A
	T_A=100℃		4.5	
	T_C=25℃		45	
	T_C =100℃		28	
Pulsed Drain Current [A]		I_{DM}	180	A
Avalanche energy [B]		EAS	90	mJ
Total Power Dissipation [C]	T_A=25℃	P_D	2.5	W
	T_A=100℃		1	
	T_C=25℃		73	
	T_C =100℃		29	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient [D]	Steady-State	$R_{\theta JA}$	40	50	℃/W
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	1.4	1.7	

■ **Ordering Information** (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJD45G10AQ	F1	YJD45G10A	2500	/	25000	13”Reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V	-	-	1	μA
		V_{DS}=100V, V_{GS}=0V, Tj=150℃	-	-	100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.0	1.8	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=22.5A	-	14	17	mΩ
		V_{GS}=4.5V, I_D=20A	-	17	21.5	
Diode Forward Voltage	V_{SD}	I_S=22.5A, V_{GS}=0V	-	0.9	1.2	V
Maximum Body-Diode Continuous Current	I_S		-	-	45	A
Gate resistance	R_G	f=1MHz, Open drain	-	1.4	-	Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=50V, V_{GS}=0V, f=1MHz	-	1165	-	pF
Output Capacitance	C_{oss}		-	265	-	
Reverse Transfer Capacitance	C_{rss}		-	8	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V, V_{DS}=50V, I_D=22.5A	-	19	-	nC
Gate-Source Charge	Q_{gs}		-	6	-	
Gate-Drain Charge	Q_{gd}		-	3	-	
Reverse Recovery Charge	Q_{rr}	I_F=22.5A, di/dt=100A/us	-	45	-	nC
Reverse Recovery Time	t_{rr}		-	40	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DD}=50V, I_D=22.5A R_{GEN}=2.2Ω	-	40	-	ns
Turn-on Rise Time	t_r		-	12	-	
Turn-off Delay Time	$t_{D(off)}$		-	55	-	
Turn-off fall Time	t_f		-	16	-	

A. Repetitive rating; pulse width limited by max. junction temperature.
B. T_J=25℃, V_{DD}=50V, V_G=10V, R_G=25Ω, L=0.5mH, IAS=19A.
C. P_d is based on max. junction temperature, using junction-case thermal resistance.
D. The value of $R_{\theta JA}$ is measured with the device mounted on the minimum recommend pad size, in the still air environment with T_A =25℃. The maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design.

■Typical Electrical and Thermal Characteristics Diagrams

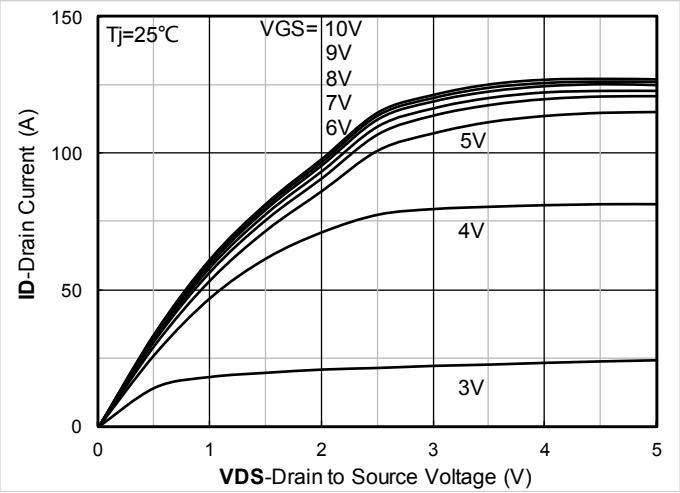


Figure 1. Output Characteristics

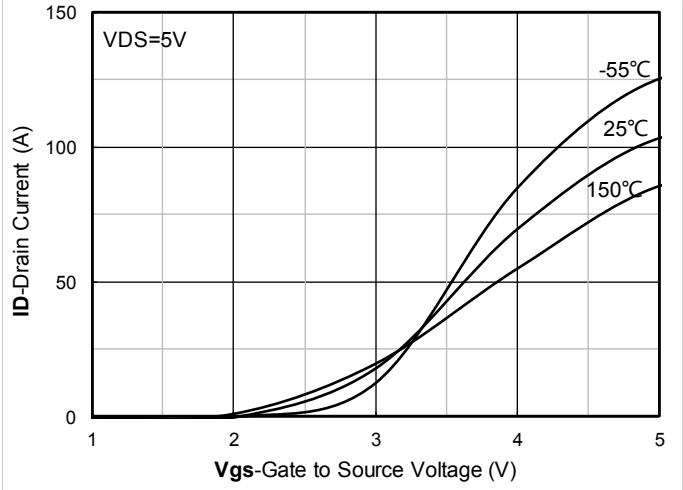


Figure 2. Transfer Characteristics

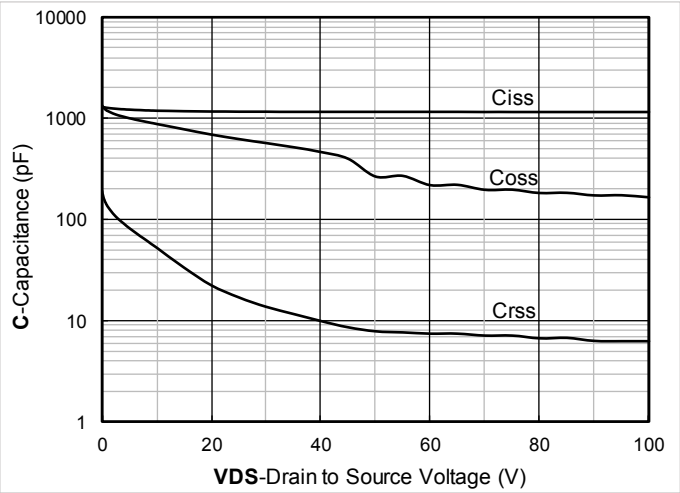


Figure 3. Capacitance Characteristics

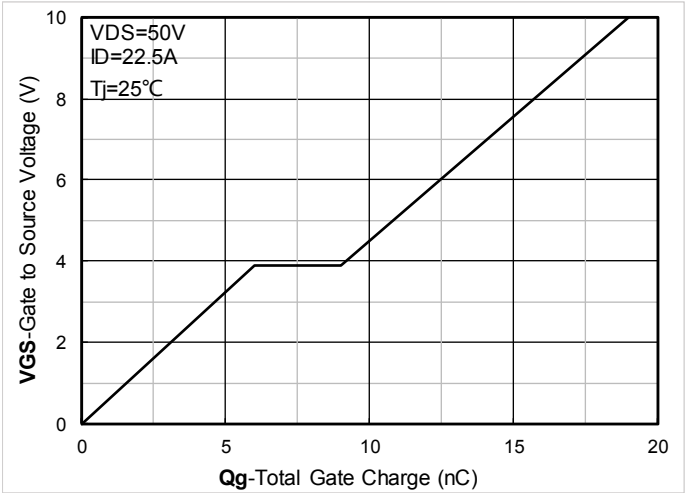


Figure 4. Gate Charge

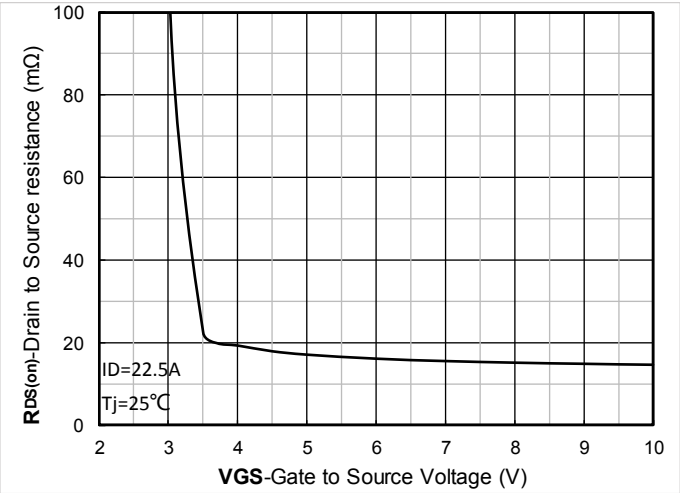


Figure 5. On-Resistance vs Gate to Source Voltage

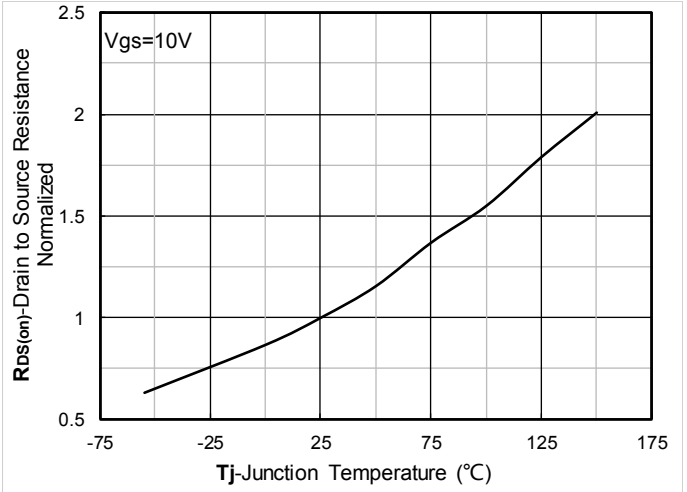


Figure 6. Normalized On-Resistance

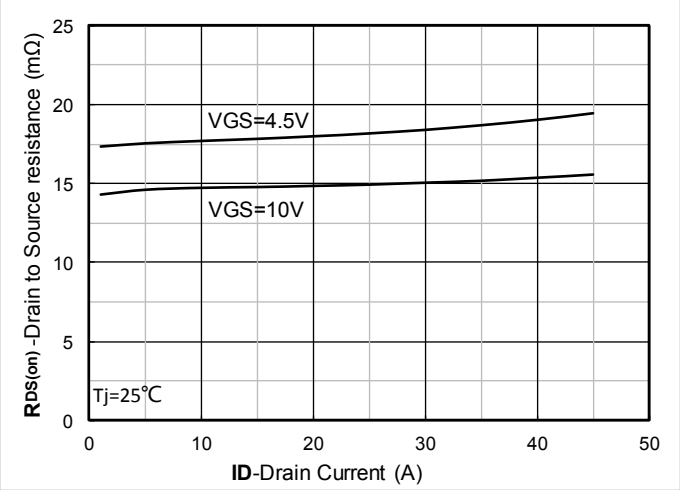


Figure 7. $R_{DS(on)}$ VS Drain Current

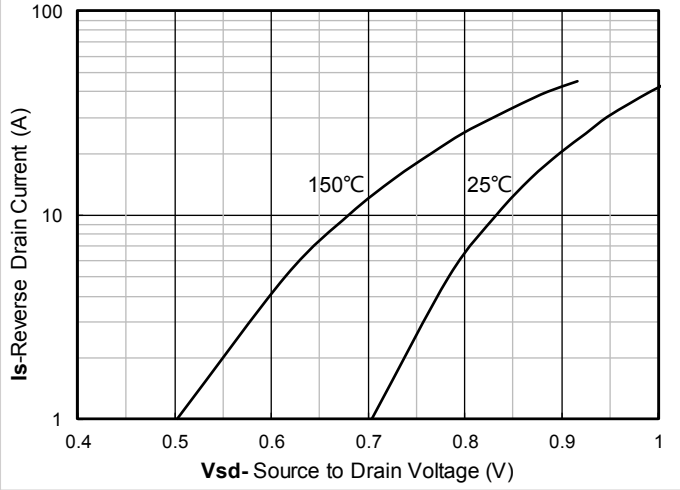


Figure 8. Forward characteristics of reverse diode

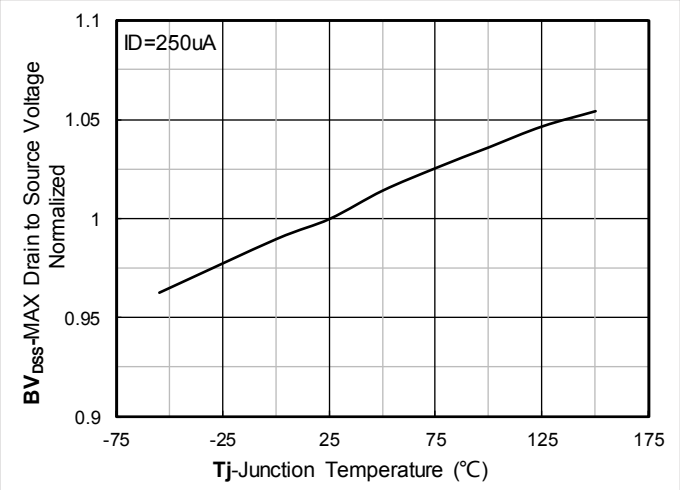


Figure 9. Normalized breakdown voltage

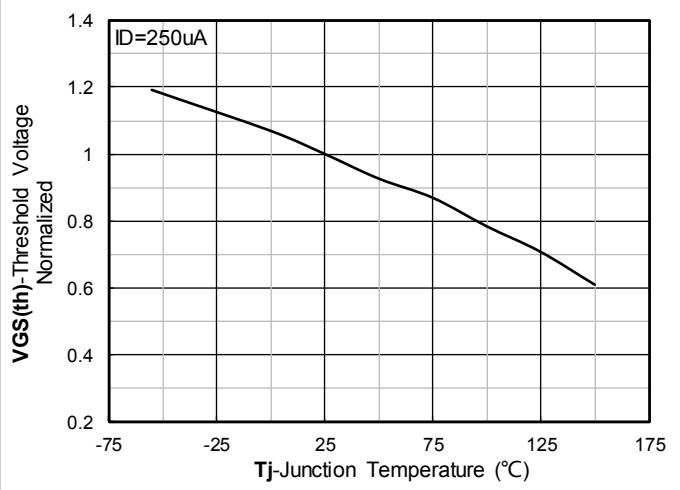


Figure 10. Normalized Threshold voltage

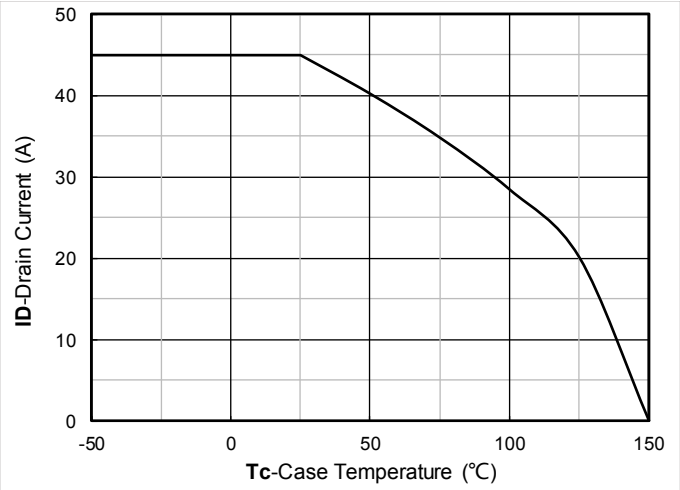


Figure 11. Current dissipation

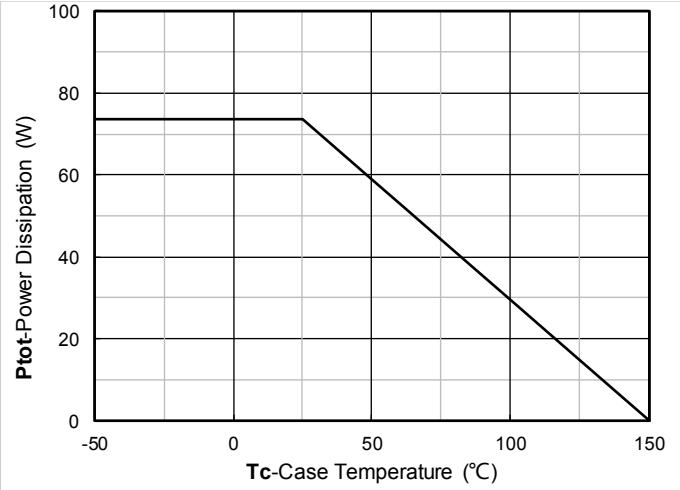


Figure 12. Power dissipation

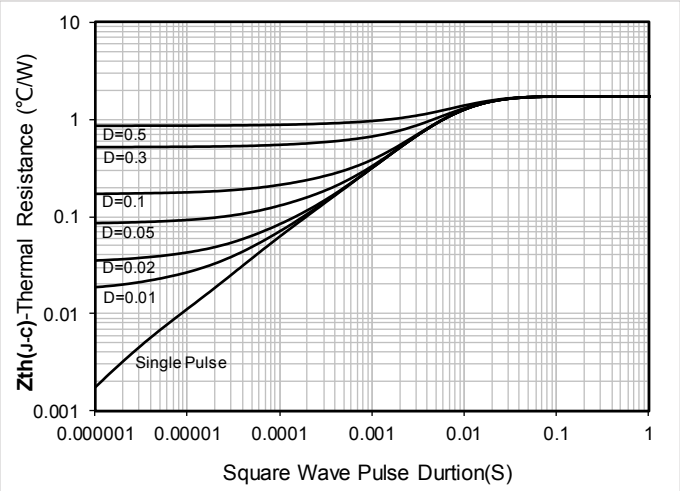


Figure 13. Maximum Transient Thermal Impedance

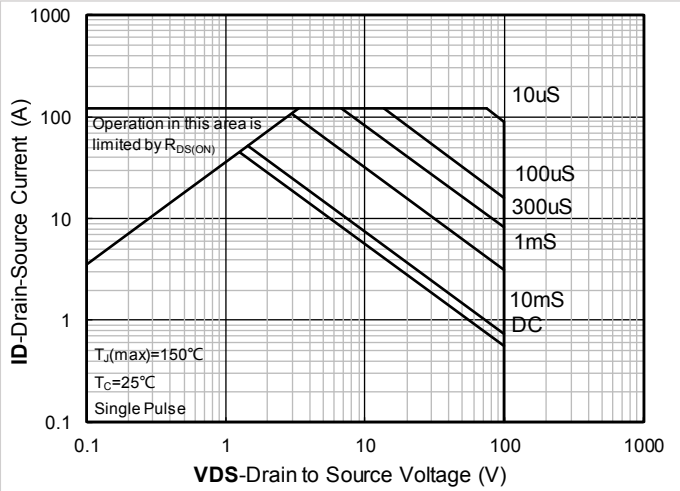


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

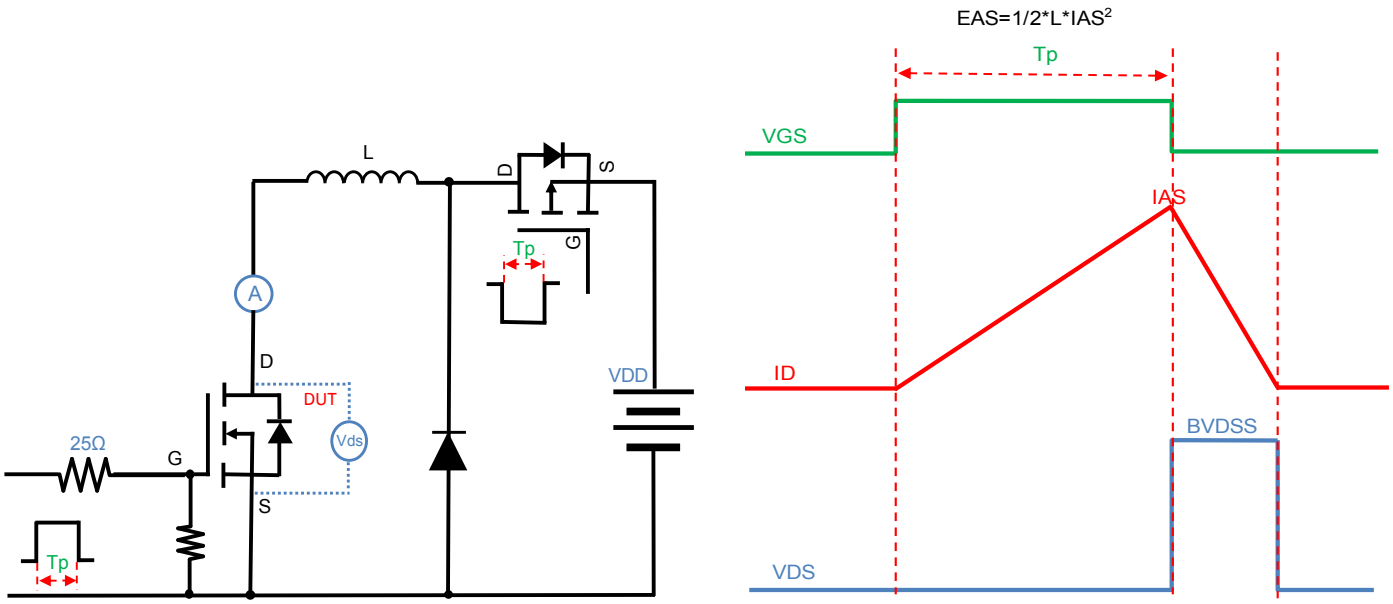


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

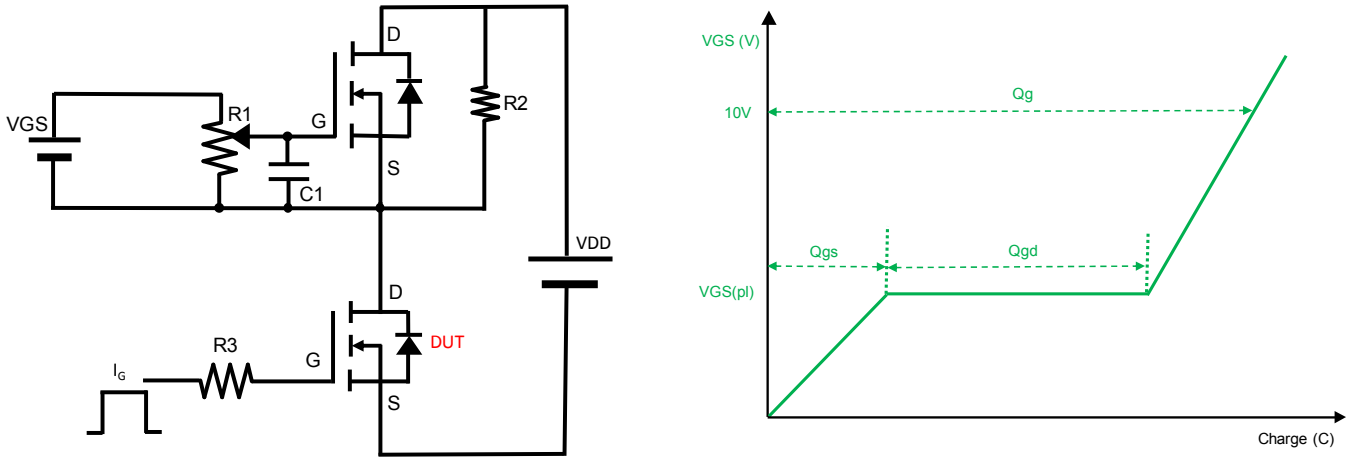


Figure B. Gate Charge Test Circuit & Waveform

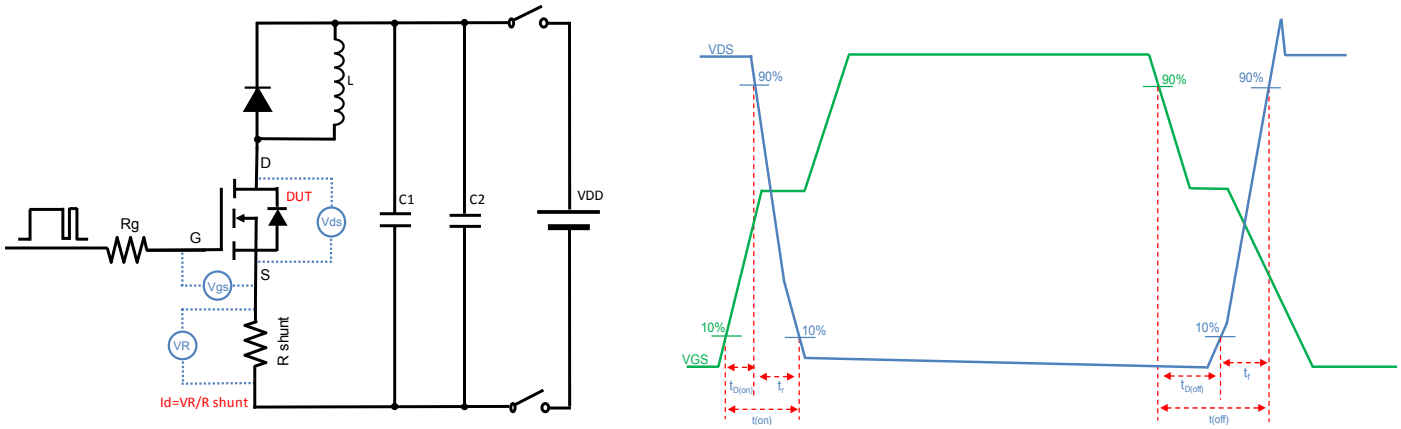


Figure C. Resistive Switching Test Circuit & Waveform

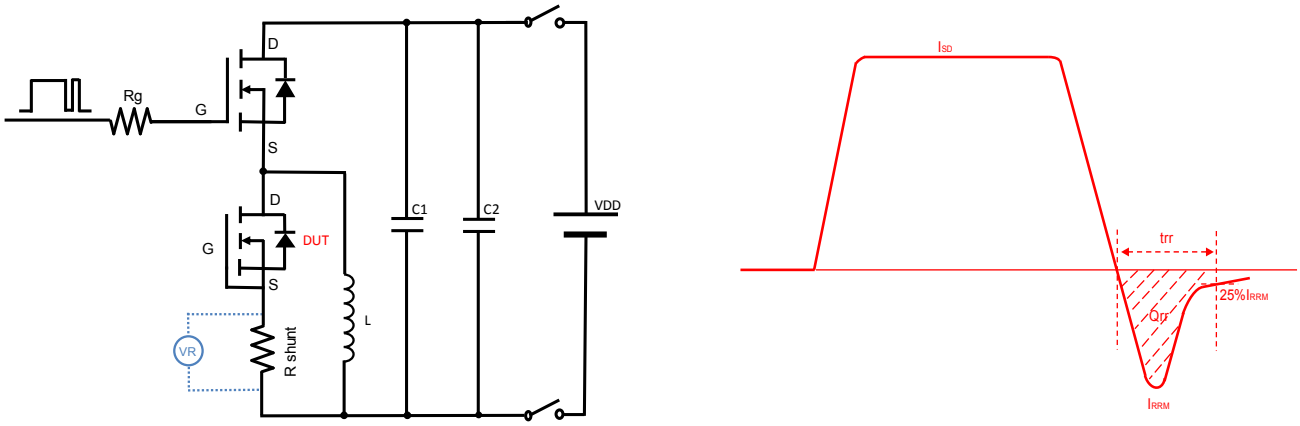
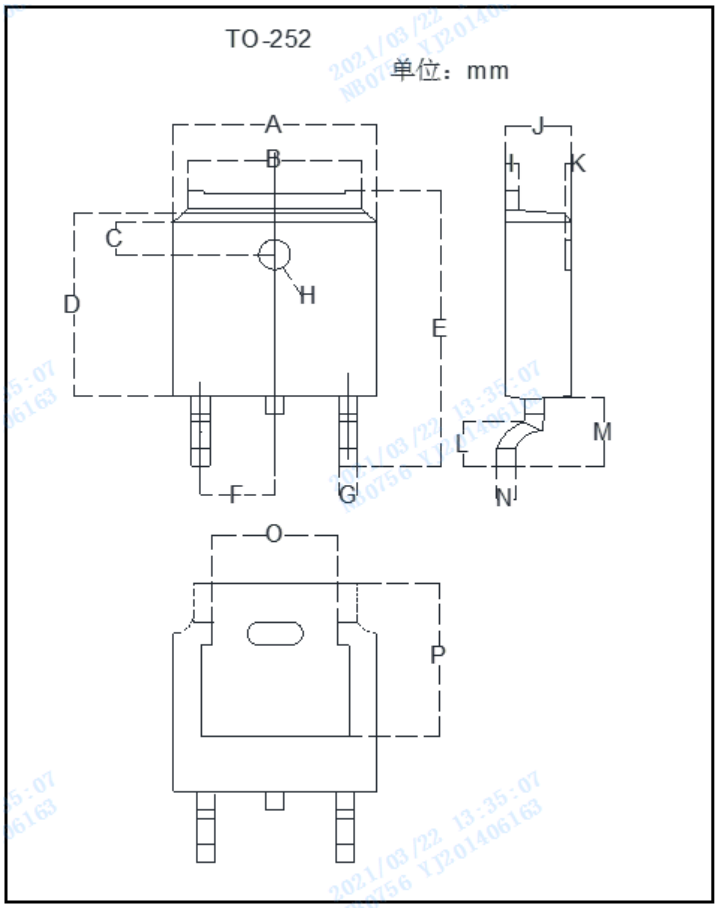


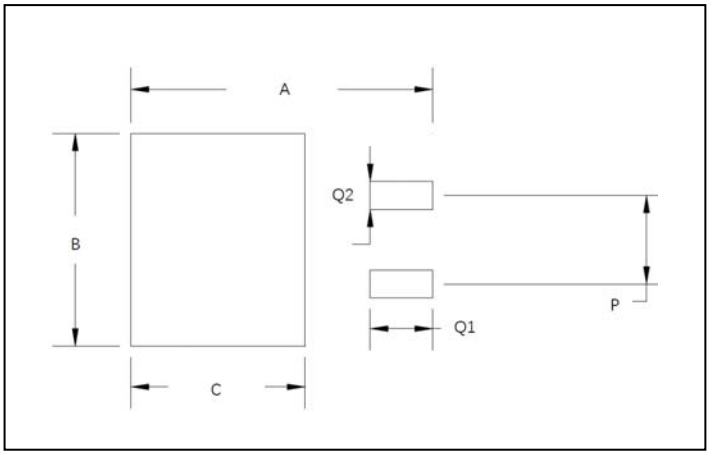
Figure D. Diode Recovery Test Circuit & Waveform

■ TO-252 Package information



DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	0.256	0.264	6.50	6.70	
B	0.201	0.215	5.10	5.46	
C	0.055	0.071	1.40	1.80	
D	0.236	0.244	6.00	6.20	
E	0.394	0.409	10.00	10.40	
F	0.085	0.093	2.17	2.37	
G	0.026	0.034	0.66	0.86	
H	Φ0.041	Φ0.531	Φ1.050	Φ1.350	
I	0.018	0.023	0.46	0.58	
J	0.087	0.094	2.20	2.40	
K	0.000	0.012	0.00	0.30	
L	0.035	0.090	0.89	2.29	
M	0.107	0.121	2.73	3.08	
N	0.017	0.023	0.43	0.58	
O	0.165	0.195	4.20	4.95	
P	0.203	0.215	5.15	5.45	

■ Suggested Pad Layout



Dim	Millimeters
A	11.4
B	6.74
C	6.23
P	4.56
Q1	2.28
Q2	1.52